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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,169	09/20/2005	Yukio Kadowaki	2271/75151	5260

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EXAMINER	
COUSO, JOSE L	

ART UNIT	PAPER NUMBER
2624	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,169	KADOWAKI, YUKIO	
	Examiner	Art Unit	
	Jose L. Couso	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/20/05,11/4/05,8/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakuyama et al. (U.S. Patent No. 6,315,651).

With regard to claim 1, Sakuyama et al. ('651) describes accepting the inclusion information of the code blocks in a predetermined sequence in units of code blocks amounting to a number which is smaller than a number of code blocks of sub-bands in all levels (refer for example to column 6, lines 32-43); and immediately generating and outputting TAG information corresponding to the accepted inclusion information (refer for example to column 6, lines 44-50).

As to claim 2, Sakuyama et al. ('651) describes wherein the first step inputs the inclusion information of the code blocks of all level-2 and level-3 sub-bands, the inclusion information of all code blocks of a level-1 sub-band 1HL, the inclusion information of all code blocks of a level-1 sub-band 1LH, and the inclusion information of all code blocks of a level-1 sub-band 1HH, in a predetermined sequence (see figure 2 and refer for example to column 5, lines 46-58).

In regard to claim 3, Sakuyama et al. ('651) describes accepting data of numbers of zero-bit-planes in a predetermined sequence in units of code blocks amounting to a number which is smaller than a number of code blocks of sub-bands of all levels, the zero-bit-planes being bit-planes in which all significant bits of the code blocks in each of the sub-bands are zero (refer for example to column 8, lines 43-61); and immediately generating and outputting ZERO-TAG information corresponding to the accepted numbers of zero-bit-planes, according to the JPEG2000 standard (refer for example to column 8, lines 43-65).

With regard to claim 4, Sakuyama et al. ('651) describes wherein in the third step inputs the data of the number of zero-bit-planes of the code blocks of all level-2 and level-3 sub-bands, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HL, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1LH, and the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HH, in a predetermined sequence (refer for example to column 8, lines 24-42).

As to claim 5, Sakuyama et al. ('651) describes accepting data of the numbers of zero-bit-planes in a predetermined sequence in units of code blocks amounting to a number which is smaller than a number of code blocks of sub-bands of all levels (refer for example to column 6, lines 32-43); and immediately generating and outputting ZERO-TAG information corresponding to the accepted numbers of zero-bit-planes (refer for example to column 6, lines 44-50).

In regard to claim 6, Sakuyama et al. ('651) describes wherein the first step inputs the data of the number of zero-bit-planes of the code blocks of all level-2 and level-3 sub-bands, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HL, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1LH, and the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HH, in a predetermined sequence (see figure 2 and refer for example to column 5, lines 46-58).

With regard to claim 7, Sakuyama et al. ('651) describes a TAG information analyzing circuit to generate TAG information based on inclusion information which indicates an existence of significant data in code blocks for each of sub-bands, according to JPEG2000 standard (see figure 1, element 16 and refer for example to column 6, lines 44-50), the TAG information analyzing circuit accepting the inclusion information of the code blocks in a predetermined sequence in units of code blocks amounting to a number which levels, and immediately generating and outputting TAG information corresponding to the accepted inclusion information (see figure 1, element 16 and refer for example to column 6, lines 44-67).

As to claim 8, Sakuyama et al. ('651) describes wherein the TAG information analyzing circuit inputs the inclusion information of the code blocks of all level-2 and level-3 sub-bands, the inclusion information of all code blocks of a level-1 sub-band 1HL, the inclusion information of all code blocks of a level-1 sub-band 1LH, and the inclusion information of all code blocks of a level-1 sub-band 1HH, in a predetermined sequence (see figure 2 and refer for example to column 5, lines 46-58).

In regard to claim 9, Sakuyama et al. ('651) describes a ZERO-TAG information analyzing circuit to generate ZERO-TAG information based on data of numbers of zero-bit-planes in which all significant bits of code blocks in each of sub-bands are zero, according to JPEG2000 standard, the ZERO-TAG information analyzing circuit accepting data of numbers of zero-bit-planes in a predetermined sequence in units of code blocks amounting to a number which is smaller than a number of code blocks of sub-bands of all levels (see figure 1, element 16 and refer for example to column 8, lines 43-61), and immediately generating and outputting ZERO-TAG information corresponding to the accepted numbers of zero-bit-planes (see figure 1, element 16 and refer for example to column 8, lines 43-65).

With regard to claim 10, Sakuyama et al. ('651) describes wherein the ZERO-TAG information analyzing circuit inputs the data of the number of zero-bit-planes of the code blocks of all level-2 and level-3 sub-bands, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HL, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1LH, and the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HH, in a predetermined sequence (refer for example to column 8, lines 24-42).

As to claim 11, Sakuyama et al. ('651) describes a ZERO-TAG information analyzing circuit to generate ZERO-TAG information based on data of numbers of zero-bit-planes in which all significant bits of code blocks in each of sub-bands are zero, according to JPEG2000 standard, the ZERO-TAG information analyzing circuit accepting data of the numbers of zero-bit-planes in a predetermined sequence in units

of code blocks amounting to a number which is smaller than a number of code blocks of sub-bands of all levels (see figure 1, element 16 and refer for example to column 8, lines 43-61), and immediately generating and outputting ZERO-TAG information corresponding to the accepted numbers of zero-bit-planes (see figure 1, element 16 and refer for example to column 8, lines 43-65).

In regard to claim 11, Sakuyama et al. ('651) describes wherein the ZERO-TAG information analyzing circuit inputs the data of the number of zero-bit-planes of the code blocks of all level-2 and level-3 sub-bands, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HL, the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1LH, and the data of the number of zero-bit-planes of all code blocks of a level-1 sub-band 1HH, in a predetermined sequence (see figure 2 and refer for example to column 5, lines 46-58).

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sano et al., Yano et al., Suino et al., Sakuyama et al. ('664) and Nomizu et al. all disclose systems similar to applicant's claimed invention.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose L. Couso whose telephone number is (571) 272-7388. The examiner can normally be reached on Monday through Friday from 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella, can be reached on (571) 272-7778. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jose L. Couso/
Primary Examiner, Art Unit 2624
June 25, 2008